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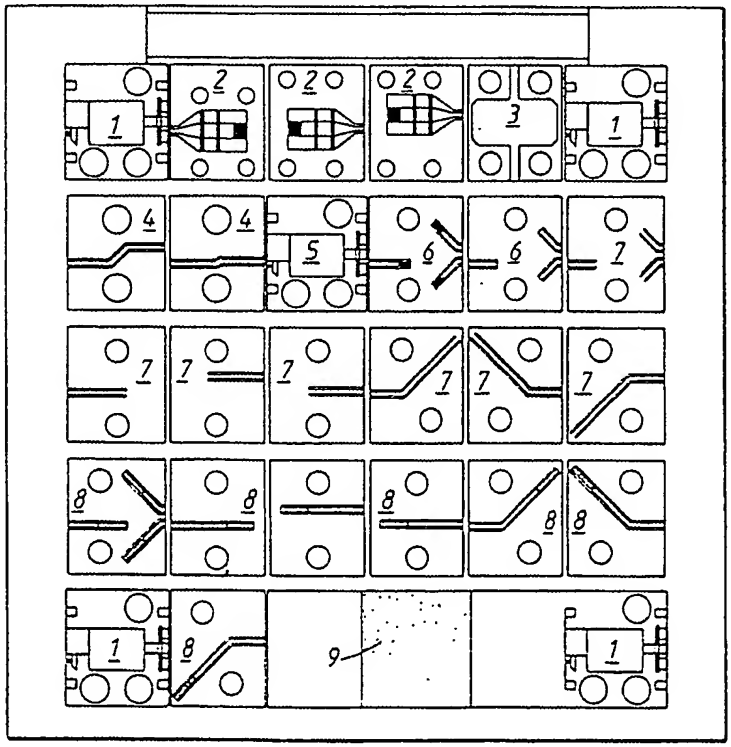
(54) Title: CALIBRATION APPARATUS FOR INTEGRATED CIRCUITS



(57) Abstract

Apparatus for calibrating an integrated circuit test system comprises a substrate having a substantially planar array of thin film components (1-9) formed thereon. The components are provided with contact pads which, for each component, have a spacing which enable the components to be engaged by the tip of a coplanar waveguide probe of the test system. Such apparatus permits error correction to be achieved under computer control, resulting in scatter parameter measurements to be made with reference planes at the tips of the probe, obviating the need for sophisticated but error prone de-embedding techniques.

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Calibration Apparatus for Integrated Circuits

The present invention relates to calibration apparatus for the automated on-wafer testing of integrated circuits and in particular for the automated on-wafer testing of Gallium Arsenide (Ga As) integrated circuits.

In order to minimise costs and timescales in the production of monolithic microwave integrated circuits, it is desirable to measure the microwave performance of an integrated circuit (IC) on-wafer prior to dicing the wafer into individual chips. A means of transferring the microwave signals from the coaxial media of the test equipments to the coplanar medium of the IC radio frequency connecting pads by low-loss, low voltage standing wave ratio (VSWR) probes is described in UK patent application No. 8511169, the contents of which is specifically incorporated herein by reference. The usefulness of such probe systems, however, is dependent on the accuracy of the measurements made and, to minimise errors, it is necessary to obtain a means of calibration for the test eqipment used.

For simple gain and power measurements it is possible to characterise the probes and feeds from the test equipment for insertion loss and use this information to compensate the actual results obtained. For sensitive vector S-parameter (scatter-parameter) measurements, however, a more precise model of the imperfections between

the test equipment and the device under test must be determined.

Network analysis in a coaxial or waveguide medium is, conventially, achieved by using a wide range of calibration and verification components. By measuring a variety of such components, e.g. matched load, short circuit, open circuit etc., it is possible to construct error models for the measurement ports and thus remove the error terms from subsequent measurements. This technique is known as 8 to 12 term error and is described in "Error Models for Systems Measurements", Microwave Journal, May 1978 by J. Fitzpatrick. However, no such components are available for variable geometry microwave probe measurements and furthermore, such components would not permit an automated calibration/test procedure to be achieved, resulting in higher production costs of the devices under test.

It is an object of the present invention to provide apparatus for enabling grounded coplanar waveguide calibration of integrated circuit test equipment whereby the grounded coplanar probes used to measure the parameters of an integrated circuit under test can be utilised in the procedure for calibrating the test equipment.

Accordingly there is provided apparatus for calibrating an integrated circuit test system, the apparatus comprising a substrate having a substantially

planar array of thin film components formed thereon, at least one of the components having contact pads arranged such that they can be engaged by a coplanar waveguide probe of the integrated circuit test system.

The substrate may comprise alumina and the thin film components may comprise a resistive layer having an overlay of metallised conductors.

The resistive layer may comprise nichrome and the metallised conductors may comprise gold.

The resistive layer may be deposited to a thickness to provide a sheet resistance of 50Ω per square for the resistive layer.

Preferably, low inductance ground connections for the components are provided by via holes containing conductive meterial, such as conductive epoxy or metal.

The present invention will now be described by way of example, with reference to the accompanying drawings which illustrates an enlarged schematic plan view of apparatus in accordance with the present invention.

Referring to the drawing, the thin film components 1 to 9 are formed on an alumina substrate, typically 1 inch square, with a thin resistive layer - NiCr for example - and plated gold conductors. The resistive layer is deposited to a thickness which provides sheet resistance of 50 per square. In the example shown the components 1 to 9 comprise as follows:-

(1) 50Ω terminations for alignment check;

(2) Distribution matched loads incorporating pseudo T attenuators; as described by H.J. Finlay et al, "Design and application of precision microstrip multi-octave attenuators and loads' Proc. 6th European Microwave Conference, Rome 1976.

(3) Short circuits;

(4) Through lines; to provide 50Ω transmission lines;

(5) 50Ω terminations for isolation measurement, to permit termination of both probes used in the IC test procedure simultaneously.

(6) Mismatch terminations;

(7) Offset short circuits; low inductance short circuits displaced by a length of 50Ω transmission line;

(8) Offset open circuits; low inductance open circuits displaced by a length of 50Ω transmission line;

(9) Large test cell to determine sheet resistivity;

The components 1 to 9 achieve low inductance local grounding by the use of via holes which may be filled with conductive material, such as conductive epoxy or metal or a metal plating on the wall of the via holes.

The components are arranged to have the same width as the IC to be tested to remove the need for adjustment

of the measuring probes between calibration and measurement and to permit auto-stepped execution of the calibration procedure. The particular example illustrated is designed for an IC having one input and two output RF ports, but other designs may be used for alternative input/output port combinations.

Calibration using such a substrate allows the use of error correction under computer control resulting in S-parameter measurements with reference planes at the probe tips, i.e. the IC RF contact pads. This removes the need for sophisticated but error-prone de-embedding techniques and is particularly valuable in individual IC component element characterisation.

Furthermore, the use of integrated calibration components as described above facilitates and enhances the quality of measurements made using the microwave probe system thereby providing a valuable tool in monolithic microwave circuit production.

It can be seen, therefore, that considerable advantages can be achieved with the apparatus of the present invention, leading to low unit cost for the tested IC components.

Although the present invention has been described with respect to a particular embodiment it should be understood that modification may be effected within the scope of the invention.

CLAIMS

1. Apparatus for calibrating an integrated circuit test system, the apparatus comprising a substrate having a substantially planar array of thin film components formed thereon, at least one of the components having contact pads arranged such that they can be engaged by a coplanar waveguide probe of the integrated circuit test system.

2. Apparatus according to claim 1 wherein the substrate comprises alumina and the thin film components comprise a resistive layer having an overlay of metallised conductors.

3. Apparatus according to claim 2 wherein the resistive layer comprises nichrome.

4. Apparatus according to claim 2 or claim 3 wherein the metallised conductors comprise gold.

5. Apparatus according to any one of claims 2 to 4 wherein the resistive layer is arranged to have a thickness for providing a sheet resistance of 50Ω per square for the resistive layer.

6. Apparatus according to any one of the preceding

claims comprising via holes containing electrically conductive material for providing low inductance ground connections for the thin film components of the array.

7. Apparatus according to claim 6 wherein the electrically conductive material comprises conductive epoxy.

8. Apparatus according to claim 6 wherein the electrically conductive material comprises metal.

9. Apparatus according to any one of the preceding claims wherein the thin film components comprise, in any combination, a 50Ω termination for alignment check, a distribution matched load incorporating a pseudo-T attenuator, a short circuit, a through line for simulating a 50Ω transmission line, a 50Ω termination for isolation measurement, a mismatch termination, an offset short circuit, an offset open circuit and a large test cell for determining the sheet resistivity of the apparatus.

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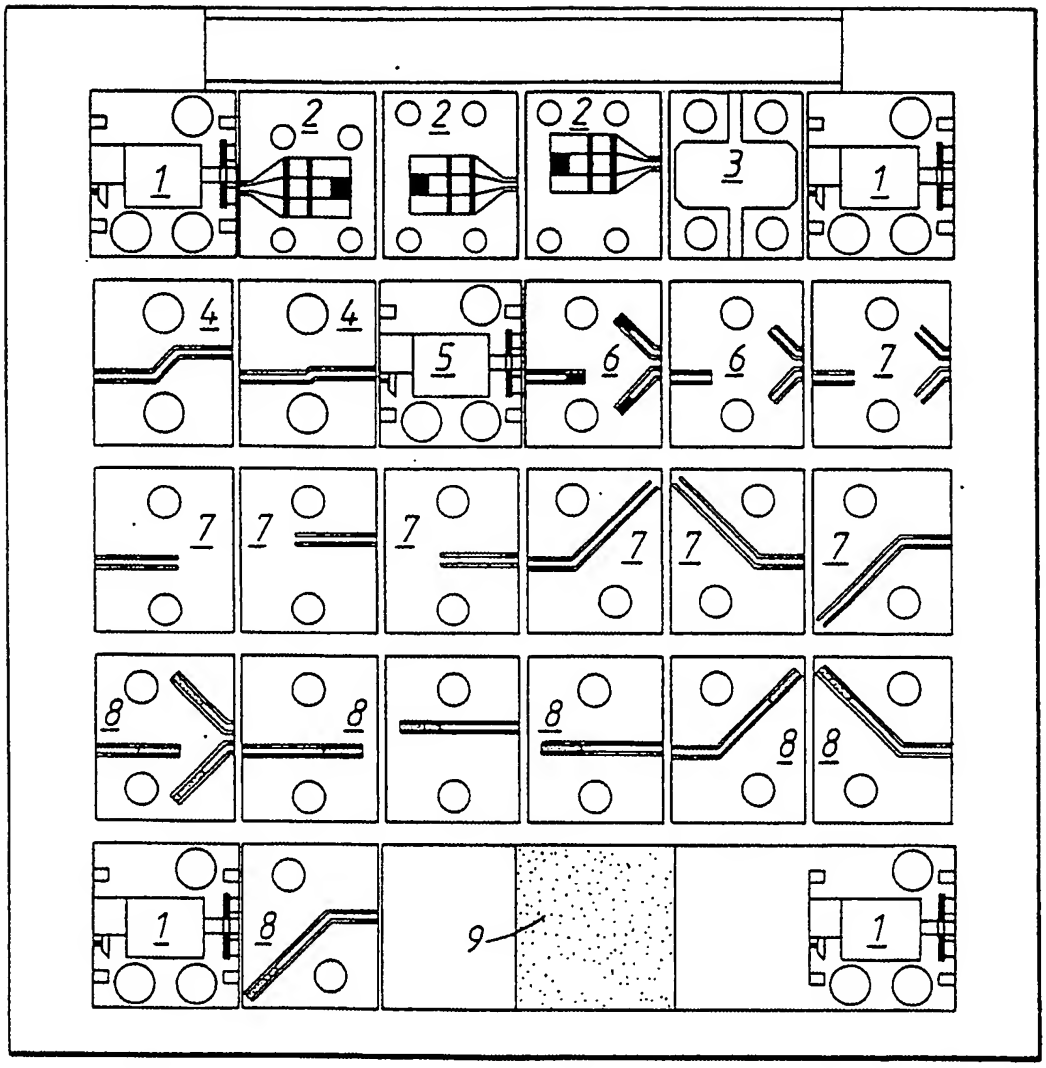

INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 86/00346

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 01 L 21/66

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with Indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	EP, A, 0128986 (SUMITOMO) 27 December 1984, see claim 1 --	1
A	New Electronics, volume 17, no. 6, March 1984, London (GB) S. Wendel et al.: "High reliability substrate attach for thin film hybrids" pages 97-100 --	1-3
A	Microwave Journal, volume 21, no. 5, May 1978, Dedham (US) J. Fitzpatrick: "Error models for systems measurement" pages 63-66 (cited in the application) --	1
A	Proceedings of the 6th European Microwave Conference, 1976, Roma (IT) H.J. Finlay et al.: "Design and applications of precision microstrip multioctave attenuators and loads", pages 692-696 (cited in the application) ---------	9

* Special categories of cited documents: [10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
19th September 1986	23 OCT 1986
International Searching Authority	Signature of Authorized Officer
EUROPEAN PATENT OFFICE	

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/GB 86/00346 (SA 13674)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 29/09/86

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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP-A- 0128986	27/12/84	JP-A-	59117155	06/07/84
		AU-A-	2275083	28/06/84
		JP-A-	59141240	13/08/84